ABSTRACT

A method and apparatus is provided for passing an N bit wide data stream between two physical devices at high speed while maintaining the coherency of the data streams during the transfer. The N bit wide data stream is transmitted in N parallel data streams on N of N+1 differential data lines. A predetermined serial sync detect pattern is transferred on the remaining differential data line, which is designated as the sync line. A sub interval clock phase is then determined for the sync line that will successfully extract the transmitted sync detect pattern during each half cycle of the clock. This sub interval clock phase compensates for differing delays in the data streams across the physical interface. All of the N+1 differential data lines are in turn designated as the sync line to determine a sub interval clock phase for each of the respective differential data lines. Data is then extracted from the N data streams by sampling at the sub interval clock phase determined for each particular data line. The number of clock cycles that pass between reception of the sync detect pattern on the sync line and reception of the sync detect pattern on the next data line designated as the sync line is counted. The counted number of clock cycles is then compared to a predetermined number of clock cycles that pass between transmission of the sync detect pattern on the respective lines to determine if any data skew of multiple clock cycles is present between the respective lines. Any detected data skew is corrected. Thus, the present invention provides an improved method and apparatus for transmitting continuous parallel data streams while the bits in the data streams maintain their relative positions when received.